SESSION X: MICROWAVE CIRCUITS

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THAM 10.1: A Monolithic GaAs FET RF Signal Generation Chip

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FULL UTILIZATION of GaAs integrated circuits in the RF and low microwave frequency range will depend upon the monolithic integration of as many functions as possible. Typical functional circuits are oscillators, mixers, amplifiers, modulators, frequency multipliers and frequency dividers. Combination of multi-function chips into compact hybrid assemblies will reduce the cost, size, and complexity of systems and instruments. GaAs IC frequency dividers[1] and broadband amplifiers[2] have been reported previously at ISSCC. An extension of this field will be offered in the description of an integrated oscillator, a doubly-balanced mixer, a phase-splitting RF amplifier, and a broadband IF amplifier combined onto a single chip to form a large part of a heterodyne signal generation system.

Figure 1 shows a block diagram of the signal-generating chip and system. The local oscillator's frequency is determined by an off-chip resonator operating on the inductive side of resonance and by on-chip varactor diodes, useful for frequency modulation and frequency-locking stabilization. An external swept-frequency oscillator provides the low-level input to a doubly-balanced mixer through a novel phase-splitting circuit. Use of a doubly-balanced mixer is required to prevent the local oscillator and RF feedthrough from saturating the IF amplifier. On/off modulation is accomplished via a modulator/buffer between the local oscillator and mixer. An on/off ratio of 30dB in IF signal is obtained. IF preamplification is provided by a single-ended on-chip amplifier[2], designed for 18dB gain into an external 200Ω load.

Figure 2 shows schematic circuit diagrams of the key on-chip circuits. The oscillator is a broadband negative resistance push-pull type whose frequency of oscillation is determined by the resonance of a parallel tank circuit formed by the on-chip capacitors and off-chip inductors; probes and wire bonds in the case of these data. Tuning is accomplished by reverse biasing the process-inherent Schottky diodes which exhibit an abrupt tuning characteristic ($C \propto V^{-1/2}$). The varactor diodes on this chip are designed with 4μm-wide interdigitated fingers for a computed Q of 20 at 5GHz. Varactor diodes are also used as coupling and bypass capacitors on this chip. Figure 3 shows the tuning characteristic of this oscillator with a particular off-chip bond wire inductor. The governing non-linearity for this push-pull oscillator is normally class C operation due to large-signal overdrive of the amplifying FETs. In this design, the unique variable clipping property of an FET driven differentially at drain and source modes can be used to regulate oscillator amplitude or to turn it off. Note that the operating principle is variable common-gate conduction threshold, not variable resistance.

The doubly-balanced mixer of Figure 2*b* is essentially a variable-gain amplifier stage in which the gain-modulating function is provided by FET variable resistors. The ac ground return for these switches guarantees nearly zero-volt drain-to-source bias which minimizes LO feedthrough. Further supression of LO and RF feedthrough is provided by parallel operation of 180° out-of-phase mixers, the active circuit equivalent of double-balancing. The voltage conversion efficiency of this mixer is estimated to be −2dB, based on IF output observed after IF preamplification.

The unity-gain RF input buffer, Figure 2*c*, uses parallel common-source and common-gate input FETs to produce 0° and 180° phases, and sublinear load devices to minimize harmonic distortion.

Figure 4 shows the chip's IF output spectrum operating into an unfiltered 50Ω load with −10dBm RF input. The chip was designed to operate into a singly-terminated 200Ω characteristic impedance low-pass IF filter which suppresses RF, LO, and out-of-band spur feedthrough. The 200Ω load condition provides a nominal IF amplifier gain of 18dB as opposed to 6dB into 50Ω shown here. The observed IF response is plotted in Figure 5. The response is flat to within 3dB to approximately 1.5GHz. An RF input level of −10dBm results in an IF output with second harmonic more than 30dB below IF fundamental.

Figure 6 shows the 650μm x 600μm chip with active area of 0.14mm^2 and dc power dissipation of 330mW.

Acknowledgments

Special thanks to D. Harkins and D. Hornbuckle for their contributions to this chip, and to C. Coxen for processing it.

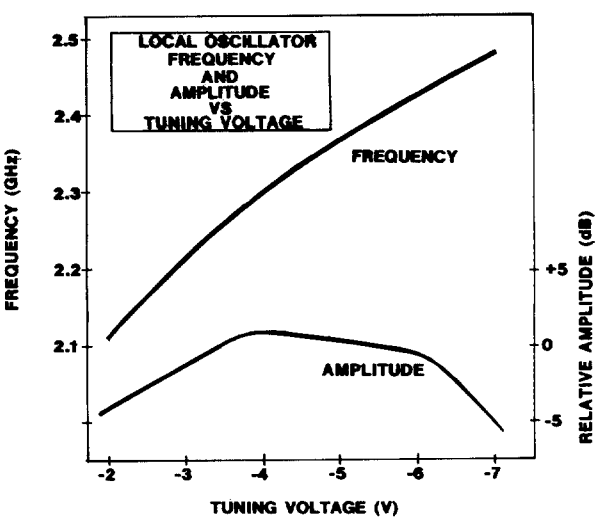

FIGURE 3—Local oscillator tuning characteristic for the particular external inductance associated with high-frequency probe and bonding wire loop. All data presented obtained with high-frequency wafer prober.

[1] Van Tuyl, R.L. and Liechti, C.A., "4GHz Frequency Division with GaAs MESFET ICs", *ISSCC DIGEST OF TECHNICAL PAPERS*, p. 198-199; Feb., 1977.

[2] Van Tuyl, R.L., "A Monolithic Integrated 4GHz Amplifier" *ISSCC DIGEST OF TECHNICAL PAPERS*, p. 72-73; Feb., 1978

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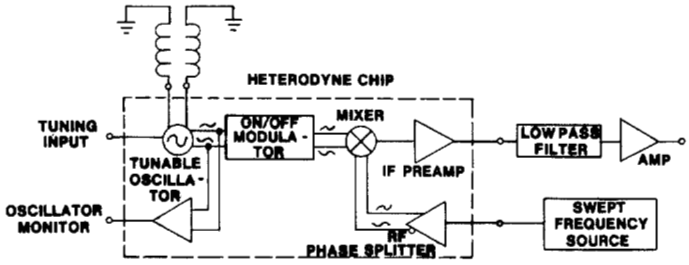


FIGURE 1—Block diagram of the heterodyne signal generation chip and associated off-chip components.

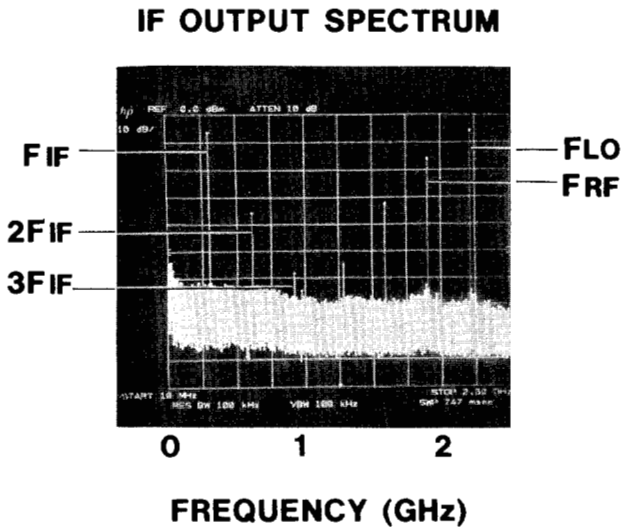


FIGURE 4

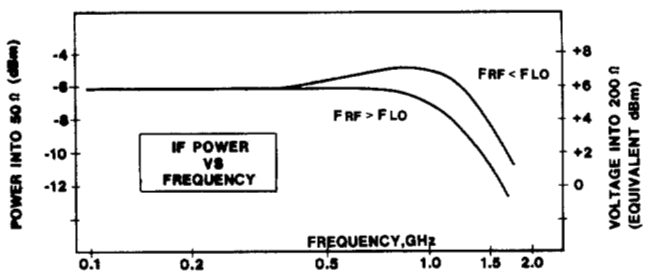
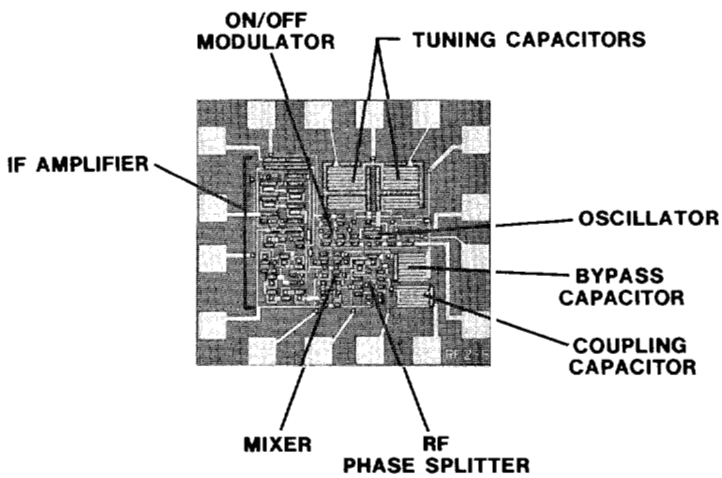


FIGURE 5



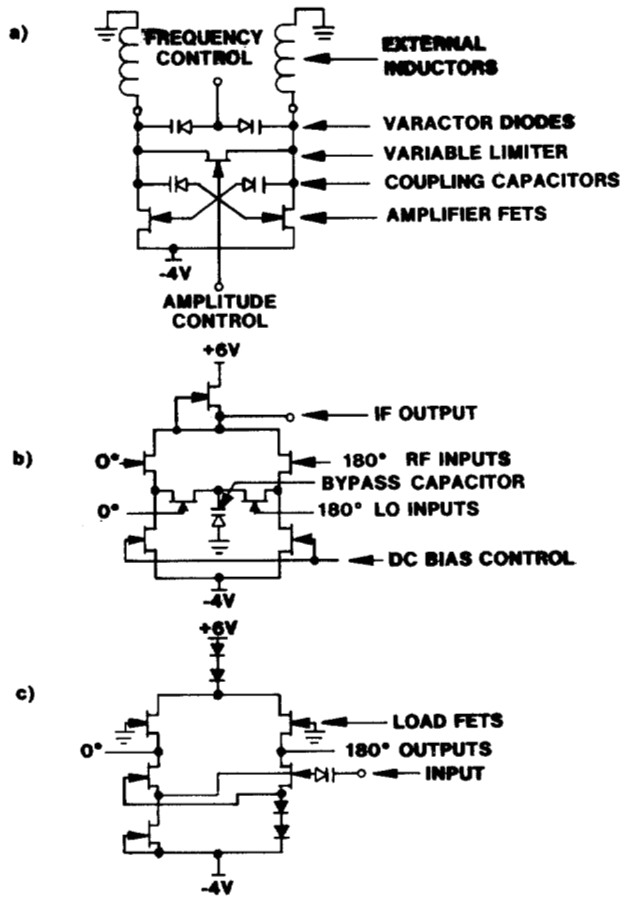


FIGURE 2—Principal circuits of the chip: (*a*) push-pull local oscillator, (*b*) doubly-balanced mixer, (*c*) phase-splitting RF input buffer.

[Left]

FIGURE 4—IF output spectrum into 50Ω load. An external 200Ω Z_o low-pass filter would filter RF and LO feedthrough and increase voltage output by 12dB.

[Left]

FIGURE 5—IF power output versus frequency. Upper curve is RF frequency less than LO frequency; lower curve is RF frequency greater than LO frequency.

[Left]

FIGURE 6—Chip photo. Active area is 400μm X 350μm; chip size is 650μm X 600μm. The circuit dissipates 300mW on-chip.